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D-band LNA in Vertical III-V Nanowire Technology

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Abstract

Simulations of a D-band three-stage LNA in a Vertical III-V nanowire technology is presented for operation in the frequency range between 130 and 175 GHz. Predictive modeling based on device scaling of measured devices together with COMSOL simulations of device parasitics has been utilized to design a virtual source VerilogA compact model for circuit simulators. The LNA achieves a gain of 21 dB at 139 GHz with a minimum noise figure of 4.7 dB using devices with f_T/f_{max}= 285/418 GHz and NF_{min}=0.76 and 2.1 dB at 50 and 150 GHz respectively. The technology is based on vertical nanowires in InAs/InGaAs grown on a silicon substrate, thereby offering a cost-effective solution.

1. INTRODUCTION

While the 5G systems are being deployed, the need for bandwidth for wireless communication between base stations is increasing. System manufacturers are currently involved in prestudies of radio links with speeds up to 100 Gb/s in the D-band between 130 and 175 GHz [1]. One of the reasons for the large interest in the D-band is that the attenuation in the atmosphere is less than 2 dB/km up to 164 GHz and increases to 3 dB/km at 174 GHz. In combination with directional antennas, low noise amplifiers in the receiver and high-power amplifiers in the transmit chain, this makes kilometer range wireless data links feasible. The vertical III-V nanowire devices shows promising predicted performance for applications in this band.

2. SEMICONDUCTOR TECHNOLOGY

The InAs/InGaAs semiconductor material has a significantly higher mobility compared to silicon. For short gate lengths, the transport mechanism of the carriers will be semi-ballistic, further improving the performance at millimeter wave frequencies. The vertical structure [2] offers low capacitive parasitics to the substrate. A simple manufacturing process flow, depicted in figure 1, with few mask steps makes the technology competitive for next generation 5G and 6G radio technology.

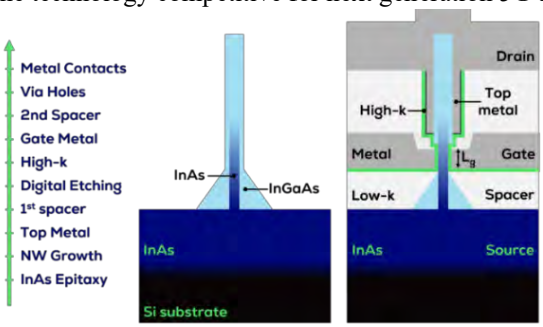

Figure 1. Vertical nanowire transistor structure

For a competitive mm-design in D-band, active devices with sufficient f_T/f_{max} are not sufficient. It is also important to have access to high performance passive components. Inductors with a Q-value of 18@150 GHz have been used throughout the design. Using the EMX electromagnetic simulator this has shown to be achievable using the present metal stack. The metal stack consists of four 0.75 µm gold layers separated by Benzocyclobutene (BCB) dielectrics with a dielectric constant ε_r equal to 2.65 and a loss tangent of 0.009 at 65 GHz [3]

3. LNA DESIGN AND SIMULATION RESULTS

Primary design targets are low noise figure and high gain, which have been achieved by cascading three stages. To reduce the noise figure, the first stage in figure 2 is implemented as a common source stage, sized as 296 nanowires divided over 8 fingers, while to improve the isolation and hereby the stability, the following two stages are designed using a cascode transistor. Due to the device properties, the common gate transistor has a large noise contribution. To optimize the real part of the input

impedance, the first stage is degenerated with a 10pH inductor. To reduce the drain voltage of the transistor in the first stage, not to violate the maximum breakdown voltage of 0.6 V, a resistor in series with the supply shifts the drain voltage down. The resonance frequencies of the interstage matching networks are offset from the D-band center frequency to increase the overall bandwidth. The input matching consists of a cascaded L-network with two sections to make the input match broadband.

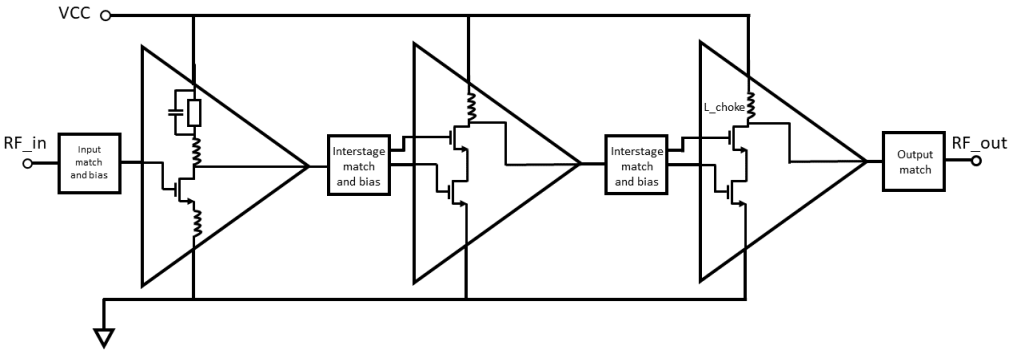

Figure 2. Architecture of the 3-stage D-band LNA

Stage 1 is biased at 9.3 mA, while stage 2 and 3 consume 6.4 and 11 mA respectively. With a 1.2 V supply voltage, the overall power consumption is 32 mW. The input 1-dB compression point of the LNA at 140 GHz, close to the maximum gain of 21 dB at 139 GHz, shown in figure 3, was simulated using the AWR Aplac simulator to -20.6 dBm. A two-tone simulation with f_1=140 GHz and f_2=141 GHz gave a third order intercept point at 139 GHz with IIP_3 equal to -10.8 dBm. From figure 3, a noise figure of 4.7 dB is obtained at 141 GHz. At the higher end of the D-band, the noise figure is significantly increased due to the reduced device gain. The 3dB bandwidth is 25 GHz. Since the received signal has a large bandwidth, having a sufficient 1dB bandwidth is also important not to distort the wanted signal. The 1dB bandwidth equals 13 GHz.

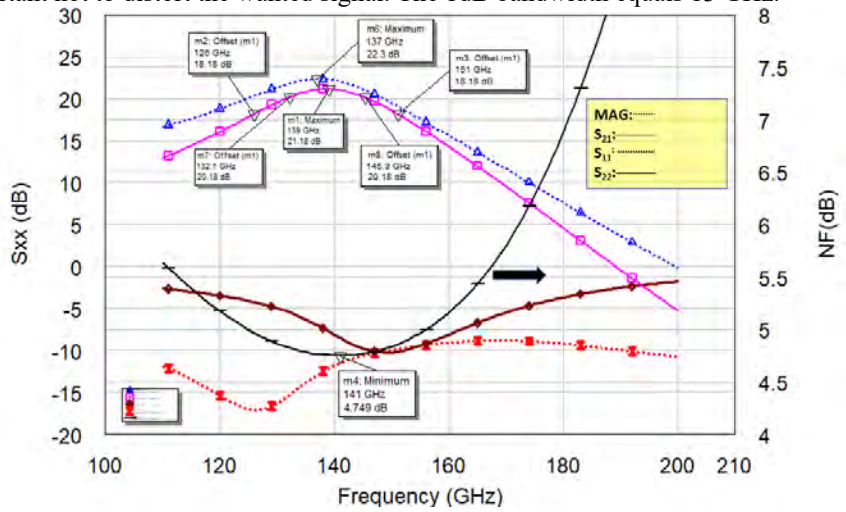

Figure 3. S-parameters and noise figure versus frequency of the D-band LNA

4. CONCLUSIONS

As demonstrated, a D-band LNA using a novel III-V nanowire device technology using a silicon substrate has been designed and simulated. The minimum NF is equal to 4.7 dB at 141 GHz. Due to the limited f_T/f_{max} for the used process generation, the performance is degraded at the upper part of the D-band. However, further process optimization is ongoing, making this an interesting technology for next generation 5G and 6G wireless backhaul.

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